

# Design, Implementation and Simulation of 24h Digital Clock Circuit Design

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**Abstract.** In this paper the design, implementation and simulation of a digital clock capable of displaying seconds, minutes and 24 hours timing is presented. The architectural design was carried out using synchronous decade counters and logic gates. The basic clock frequency signal (in hertz) that drives the clock was generated using a clock voltage source of the simulator for frequency division of the desired clock pulse. The digital clock circuit was implemented and simulated using Proteus software version 8.6 on personal computer (PC).

**Keywords.** synchronous decade counter, logic gates, logic level, clock pulse.

## 1 Introduction

There are several existing clocks in this world; analogue and digital, which one may wonder what other uses the clock may have. A digital clock is a type of clock that displays the time digitally. Instead of the rotary mechanism of electromechanical clock, it uses digital counters that count second, minute and hours. Each sixty seconds make a minute and each sixty minutes an hour connected to the output of the. After twenty four hours the clock resets and starts from initial condition. The functional unit of a digital clock is a counter that represents a second, minute or hour block. A counter [1] may be defined as a register i.e. a group of flip-flops that goes through a predetermined sequence of states upon the application of input pulses. The logic gates in a counter are connected in such a way as to produce a prescribed sequence of binary states in the register. Originally Timers were designed to fulfill a need in industry for a means of keeping time on certain devices. These timers were mechanical

devices and used clockwork mechanisms as a means of keeping a regular time. With so many tasks that must be done on scheduled manner, keeping track of time and date has become so imperative that it is now a necessity .

This research provides basic information and the fundamental use of digital circuitry and how to develop, design and implement a digital clock using synchronous decade counter and logic gate circuits. [1] [3] [4]. These tools are used to design the different parts of the clock and then implemented to create a customized clock. The clock will provide and keep track of seconds, minutes, hours, days and months information digitally and will be operated using a basic clock frequency signal in hertz generated from the clock voltage source of the simulator, and fed into the clock counters synchronously. The seconds and the minutes circuits are designed by cascaded arrangement of a divide-by-60 counter that will count from 00 to 59 and then recycle back to 00 for 60 seconds or 60 minutes count when a clock pulse is applied to their clock inputs [1]. The output is fed into the input of the minutes circuit so that for every 60 seconds the minutes counter will advance through its states from 00 to 59. Similarly, the Hours circuit section is formed by divide-by-10 and a truncated sequence divide-by-10 counter connected through the output of the minutes section such that for every 60 minutes the counter would advance through its states from 01-12 hours or 01-24 hours timing depending on the users choice of selection from a switch to affect the choice. These different sections are connected together to form the required design of the digital clock and each information provided

by them would be displayed using seven segment displays [1, 3, 4]

## 2 Methodology

To design a digital clock that has an approximate time precision with any workable clock, it is necessary to have knowledge on the basic ideas used for designing any digital system from a set of fully specified states tables or an equivalent representation of state diagram for sequential circuits or well defined truth table for combinational elements [1, 3, 4, 2]. For this design fixed function integrated circuits are used that is a synchronous decade counters and some combinational elements are utilized for proper operation. The number of counters required is determined from the number of states needed in the circuit. The design process or procedures always involves transformation of the related problems faced in sequential-circuit design into a well-articulated combinational-circuit problem for better picture of the problems involved [3]. The steps involved for these design are outlined below;

1. The word description of the circuit behavior is stated, which is accompanied by obtaining a state diagram, a timing diagram, or other related information.
2. State table is obtained from the given information about the circuit.
3. The number of states may be reduced by any simple state-reduction method if the sequential circuit can be characterized with input-output relationships independent of the number of states.
4. Binary values are assigned letter symbols for each state from the state table obtained in step 2 or 3.
5. The number of counters needed is determined and letter symbol is assigned to each.
6. From the state table, the circuit excitation, inputs and outputs characteristics are analyzed.

7. Simplification method is used to derive the circuit inputs and outputs functions where necessary.

8. Circuit diagram is obtained and implemented.

### 2.1 Design Procedures

For easier design, the general circuit of the digital clock is divided into three sub sections namely;

1. Second counter circuit section.
2. Minute counter circuit section.
3. Hours counter circuit section.

The flow chart in Figure 1 gives step by step descriptions of the process involve in designing the digital clock from the second minute and hours circuit section.

This forms the digital clock, taking into consideration that the clock pulse that drives the design clock is used from the simulators clock voltage generator at a specific frequency. They can be implemented, tested and analyze quite easily if treated individually. Each of the sub-circuit is implemented by designing logic circuits that perform its duties. Proteus 8.6 is used to design the logic circuits in this research work. Table 1 below gives the name of component and series used for this design.

**Table 1.** Components used

Name	Series
2- inputs AND gate	74HC108D
2- inputs OR gate	74HC32D
2- inputs NAND gate	74HC01D
CMOS BCD-to-7-Segment Latch Decoder	CD54HC4511
DUAL J-K FLIP-FLOPS WITH CLEAR	SN74107

### 2.1.1 4511 IC

The features of 4511 IC are :

1. Low logic circuit power dissipation
2. High current sourcing outputs (up to 25 mA)
3. Latch storage of code
4. Blanking input
5. Lamp test provision
6. Readout blanking on all illegal input combinations
7. Lamp intensity modulation capability
8. Time share (multiplexing) facility
9. Equivalent to Motorola MC14511

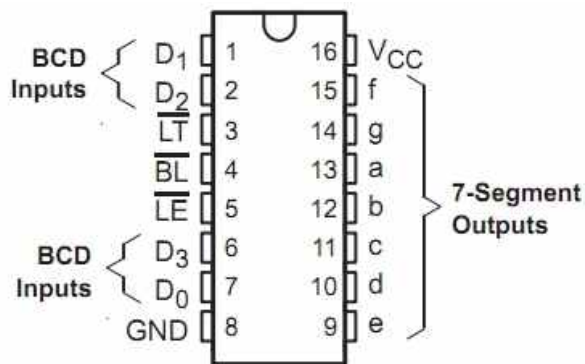


Fig. 1. 4511 pin configuration

### 2.1.2 JK74107 IC

The '107 contain two independent J-K flip-flops with individual J-K, clock, and direct clear inputs. The '107 is a positive pulse-triggered flip-flop. The J-K input data is loaded into the master while the clock is high and transferred to the slave and the outputs on the high-to-low clock transition. For these devices the J and K inputs must be stable while the clock is high.

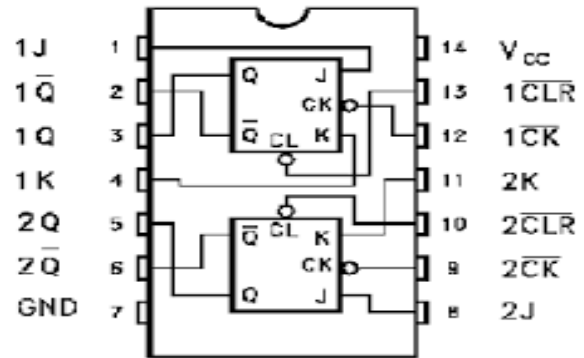
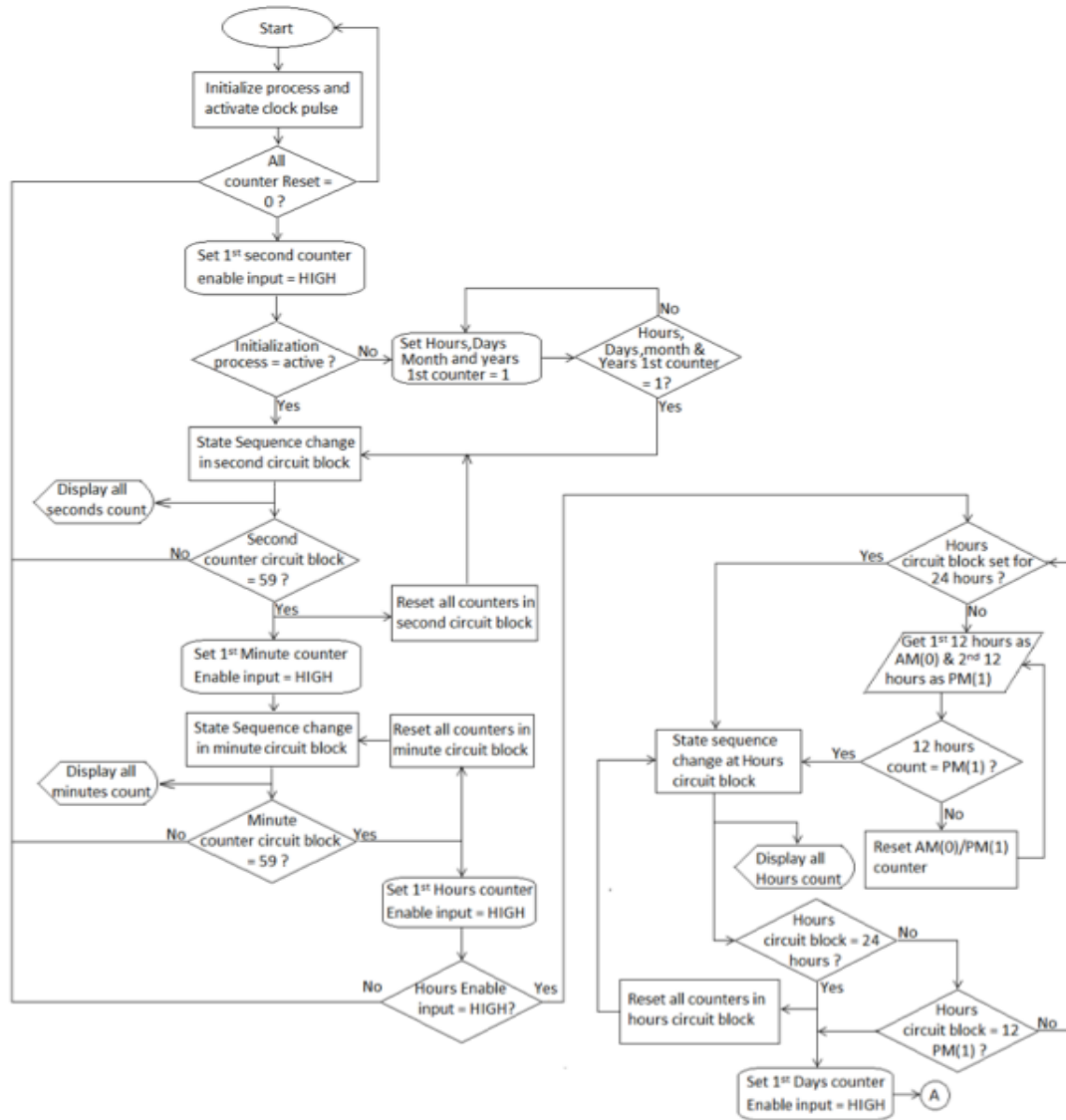


Fig. 2. JK75107 pin configuration

### 2.2 Second counter circuit section

The second counter circuit is designed and implemented by cascaded arrangements of eight dual J-K flip flop with clear as shown in Figure 2.

The asynchronous decade counters used in this paper are made using 4 dual J-K Flip Flops and NAND gates. The 1<sup>st</sup> counter (C1) is connected as a divide-by-10 counter that counts from 0 to 9 and then recycles back to 0, the 2<sup>nd</sup> counter (C2) is connected as a divide-by-6 portion of the counter that counts from 0 to 5 and then recycles back to 0. The ripple clock output ( $Q_1$  AND  $Q_3$ ) of the counter C1 is connected to the CLK input (Enable inputs) of C2 such that when C1 advances through all its states from 0 to 9, on the clock pulse that recycles it from 9 back to 0 also called the Terminal Count (TC), it output goes HIGH and hence activates the clock input of C2 to illuminates a 1 on its display [1, 3, 4]. The total count is now 10 (the 1<sup>st</sup> counter is in the zero state and the 2<sup>nd</sup> counter is in the first state). The 2<sup>nd</sup> counter (C2) remains in the first state while the 1<sup>st</sup> counter (C1) keeps advancing through its states; 1 through to 9 for count 11, 12, up to 19 and on its Terminal count (TC) the output goes HIGH again and activates the C2 to illuminates a 2 on its display for a total count of 20 (the 1<sup>st</sup> counter is now in the zero state and the 2<sup>nd</sup> counter is in the second state). This process continues, for every Terminal count of the counter C1 (0 through 9) C2 advance to the next state in its sequence until the total count is 59 before all the two counters recycles to 00 for count 60.



**Fig. 3.** Flow chart of second, minutes and hours circuit section

In general, the  $2^{nd}$  Counter (C2) is inhibited by the LOW on its Enable inputs until the  $1^{st}$  counter (C1) reaches its last or terminal state before its terminal count output goes HIGH to activate it. In other words, C1 has to go through ten complete cycles from 0 to 9 before C2 advance through one cycle. Together these counters count from 00 for 00 second, 01 second up to 59 second and then recycle to 00 for 60 second count.

The terminal count, 59 is also decoded through the AND gate to enable/allow the next Counter in the chain (minute circuit section) to sequence through it states by providing a HIGH logic level on its clock input. This HIGH logic level enables the clock input of the next Counter in the chain to set the time in the minutes circuit section as desired. However, it should be noted that the divide-by-6 portion of the  $2^{nd}$  counter (C2) is

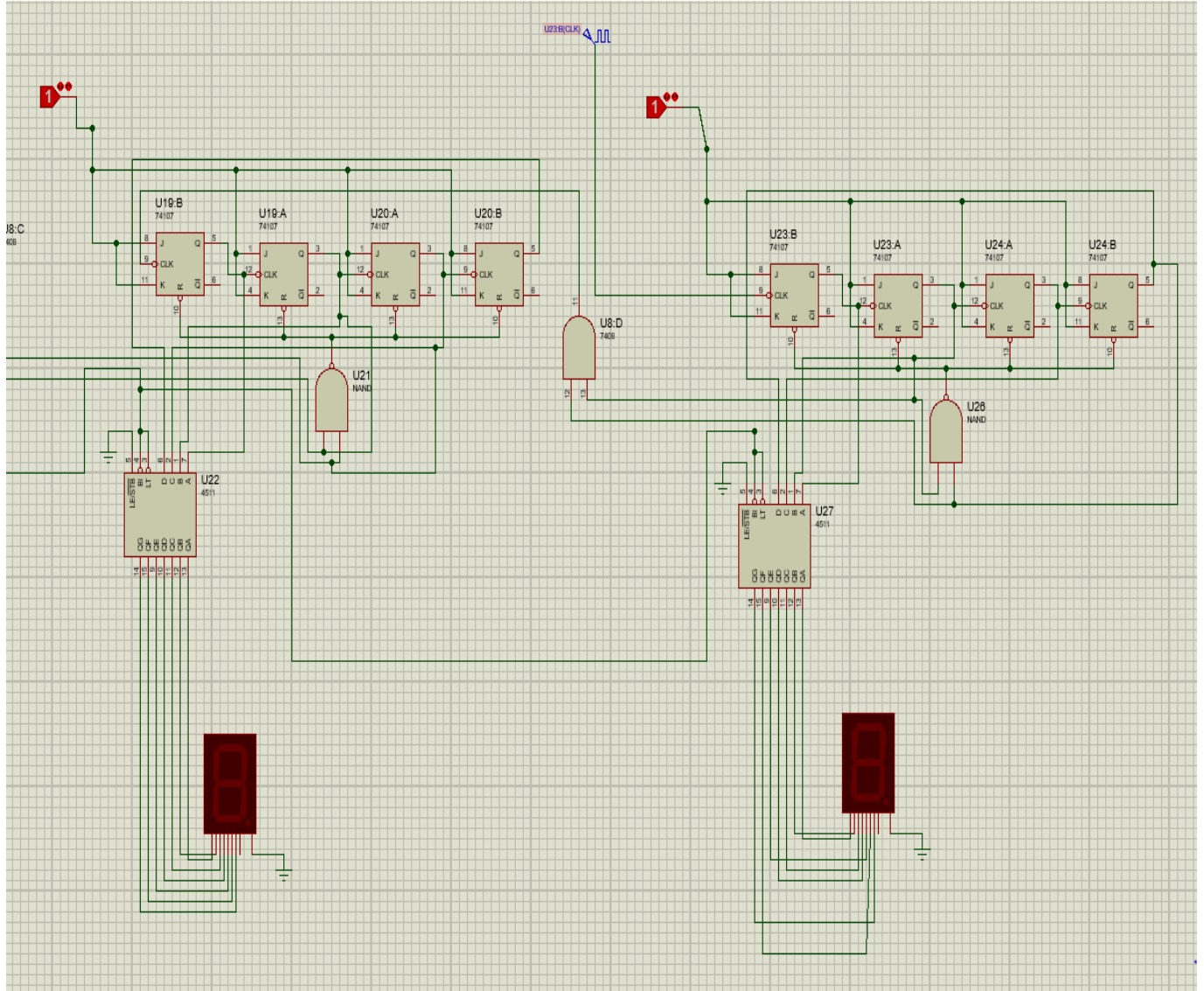


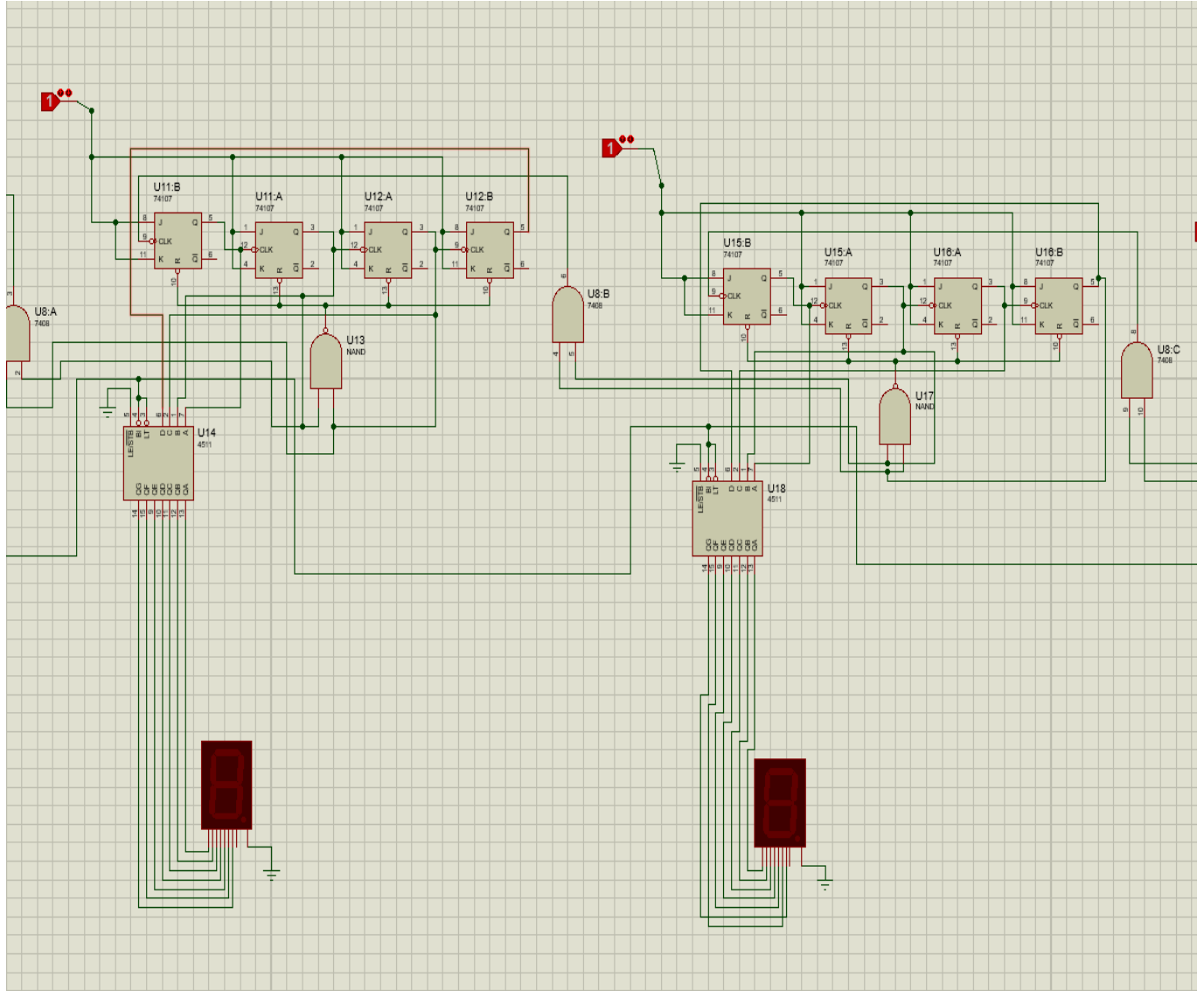
Fig. 4. Second Counter circuit

formed by decoding count 6 through the AND gate such that when the counter is in the sixth state the output of the gate becomes LOW, which in essence makes the next AND gate LOW since one of its input connected to the RESET button is LOW (when the button is not depressed). Similarly, the Clear input (CLR) of the  $2^{nd}$  counter (C2) has an Active-LOW input, hence, the LOW logic level on the output of AND gate asynchronously clear the

counters through the Clear input (CLR).

### 2.3 Minute Circuit Section

The minute circuit section is similar to the second circuit section in its operation and the process of displaying its counts as shown in Figure 3. This operational process is resulted by utilizing the counters C1 and C2, and logic gates as



**Fig. 5.** Minute Counter circuit

appropriate. However additional circuitries of logic gates are required to enable the divide-by-6 portion of the counter (C2) to have a perfect counting sequence and to enable/allow the next Counter in the chain (Hours circuit section) to sequence through it states.

### 2.4 Hour circuit section

The hours counter circuit architectural design is carried out and produce by cascaded arrangements of two 4-bit asynchronous decade counters with combination of some basic logics gates as required. The 1<sup>st</sup> and 2<sup>nd</sup> counter (C1 and C2) are connected as a divide-by-10 counter that counts from 0 to 9, however the 2<sup>nd</sup> counter is

design with additional features to exhibit different characteristic for specific timing.

A truth table is written down for these counts and a standard Boolean expression is obtained by presenting all the possible value of the resulting outputs variables using karnaugh mapping. Table 2 gives the possible values in decimal and the corresponding outputs in their equivalent 4-bit binary coded decimal (BCD) group. The timing from 13 to 19 is expressed separately likewise 20 to 24 so as to have each count with similar digit displayed from the 2<sup>nd</sup> counter C2 in one group for easier implementation and a 4-variable karnaugh mapping of each group is obtained individually. Each of the 4-bit groups are analyze keeping in mind that the first 4-bit group is displayed from the 1<sup>st</sup> counter C1 and the second 4-bit is displayed from the 2<sup>nd</sup> counter C2 as shown in Figure 4.

Hours displayed from the 2 <sup>nd</sup> counter C2 with 1 as the first digit	Hour displayed in decimal from both counters	Hours In 4-Bit BCD code displayed from the 2 <sup>nd</sup> counter C2 through its Q output				Hours In 4-Bit BCD Groups displayed from the 1 <sup>st</sup> counter C1 through its Q output			
		D	C	B	A	D	C	B	A
	13	0	0	0	1	0	0	1	1
	14	0	0	0	1	0	1	0	0
	15	0	0	0	1	0	1	0	1
	16	0	0	0	1	0	1	1	0
	17	0	0	0	1	0	1	1	1
	18	0	0	0	1	1	0	0	0
	19	0	0	0	1	1	0	0	1
Hours displayed from the 2 <sup>nd</sup> counter C2 with 2 as the first digit	20	0	0	1	0	0	0	0	0
	21	0	0	1	0	0	0	0	1
	22	0	0	1	0	0	0	1	0
	23	0	0	1	0	0	0	1	1
	24	0	0	1	0	0	1	0	0

**Fig. 6.** 4-bit group displayed from the 1<sup>st</sup> counter and 2<sup>nd</sup> counters

### 3 Conclusion and future works

In conclusion the Design of the digital clock/stopwatch was successfully carried out using synchronous counter and basic logic gates. The designed system was implemented using Proteus version 8.6. The Simulation result shows that the system functions as desired, where for every 60 second there is one minute and for every 60 minutes there is 1 hour, until the clock reach 12 hours or 24 before it cycle back to 1 hour.

Future works include :

1. Giving user choice between 12 and 24 hr clock
2. A digital clock with a date indicator that display days ,months and years using synchronous decade counters and logic gates.
3. Implement Stop watch

### References

1. **Floyd, T. L. (2011).** *Digital Fundamentals, 10/e.* Pearson Education India.
2. **Kleitz, W. (2011).** *Digital Electronics: A practical approach with VHDL.* Prentice Hall.
3. **Mano, M. M. (2002).** *Digital design.* EBSCO Publishing, Inc.
4. **Scherz, P. (2006).** *Practical electronics for inventors.* McGraw-Hill, Inc.